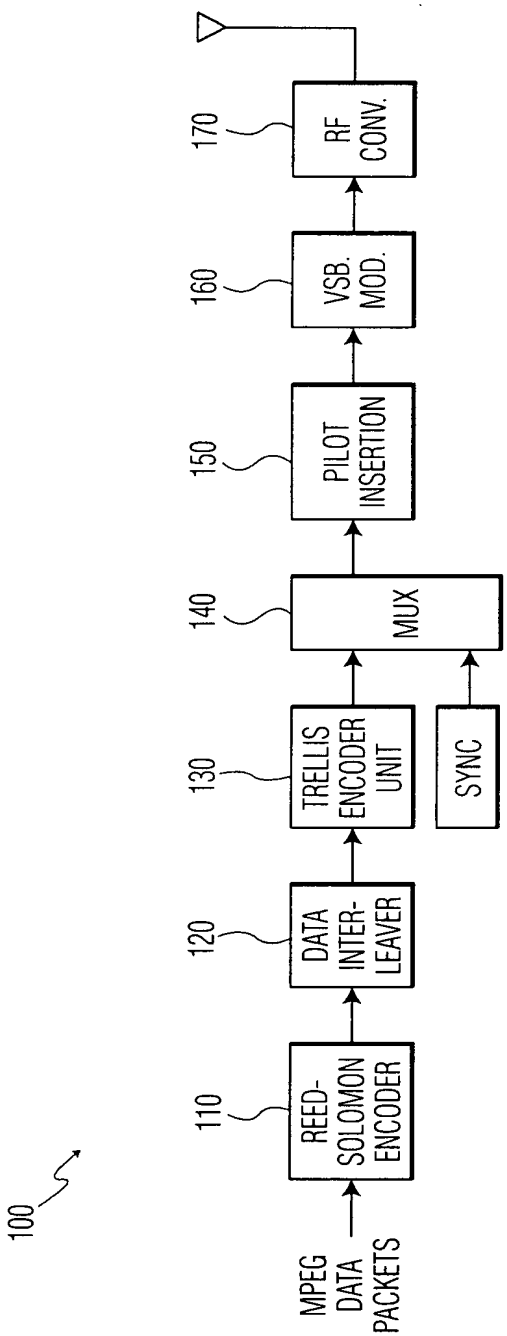


FIG. 1
PRIOR ART

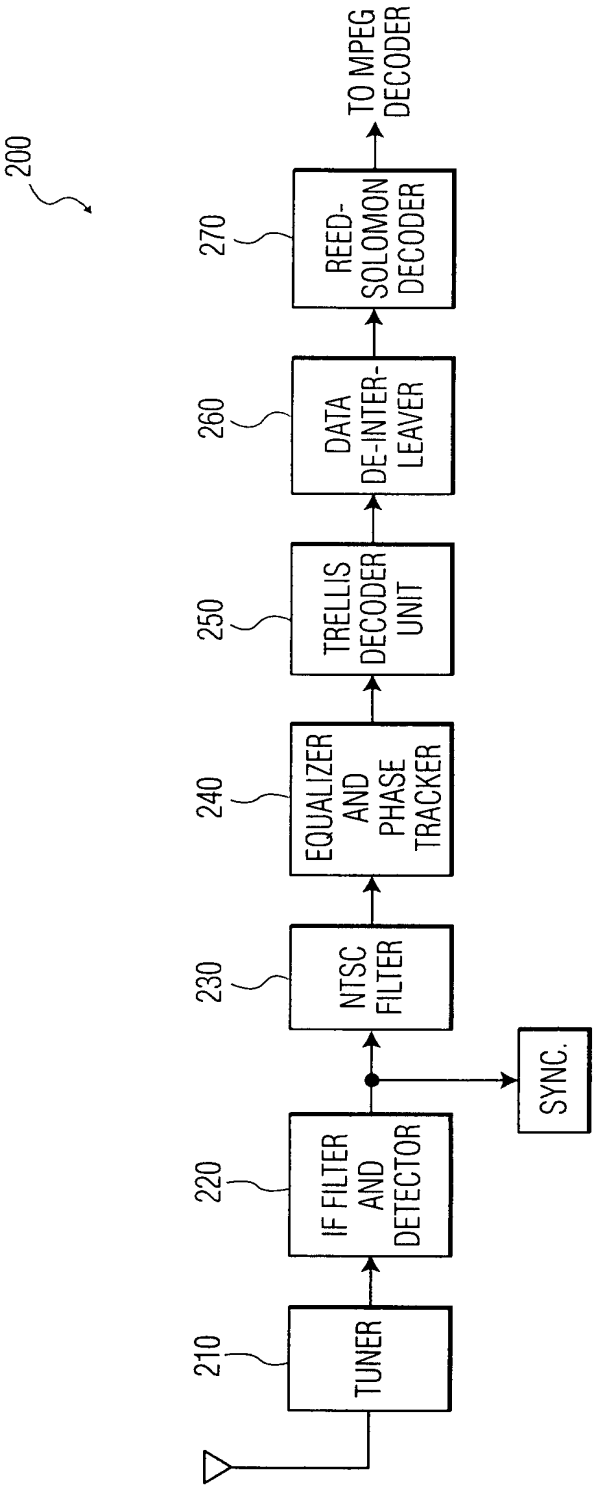


FIG. 2
PRIOR ART

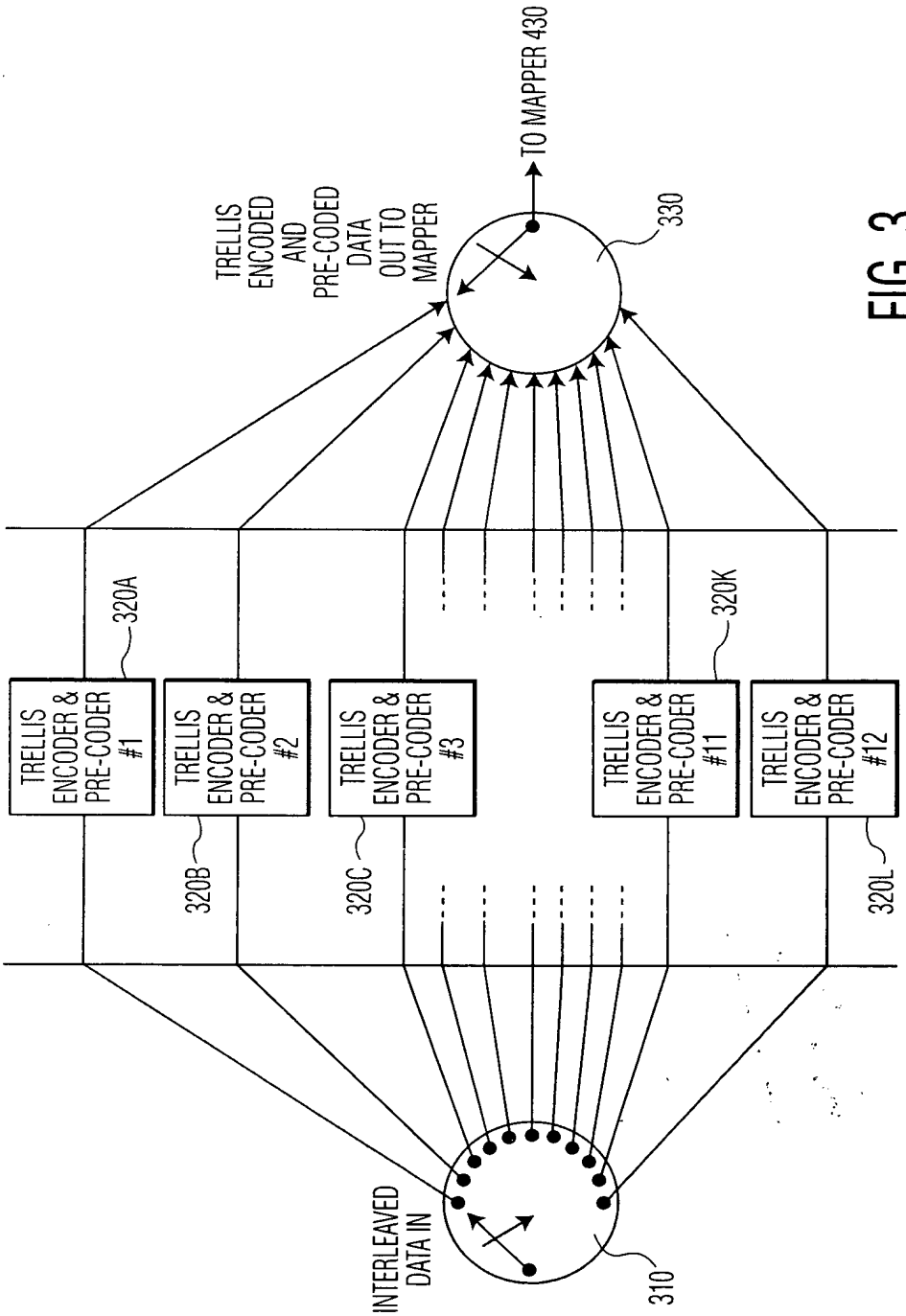


FIG. 3
PRIOR ART

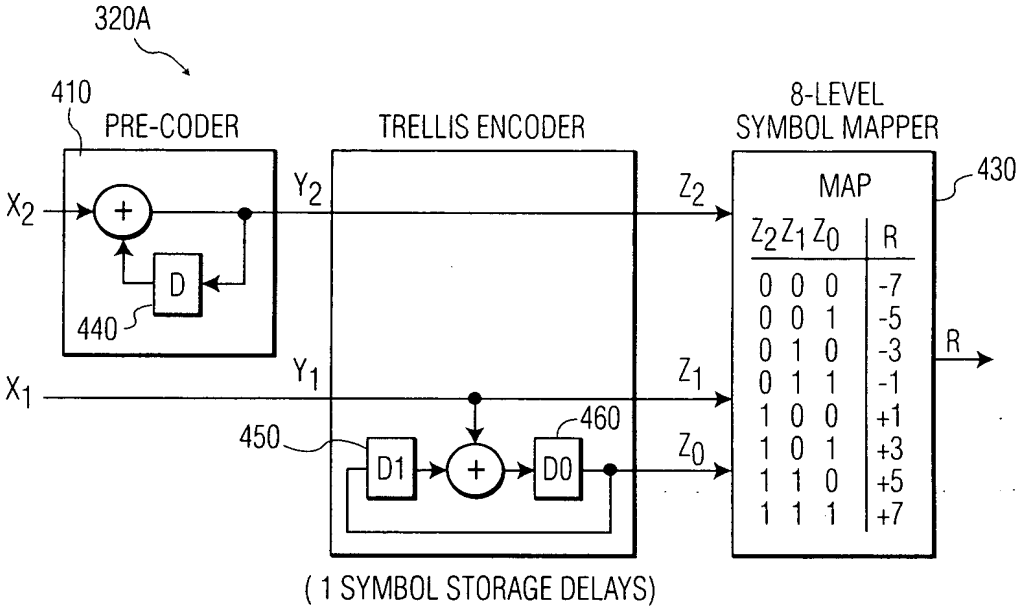


FIG. 4
PRIOR ART

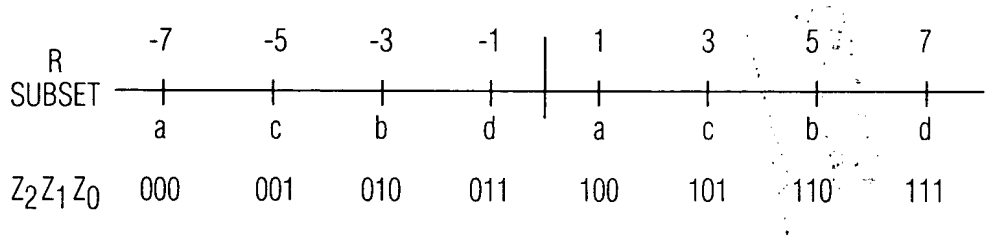


FIG. 4A
PRIOR ART

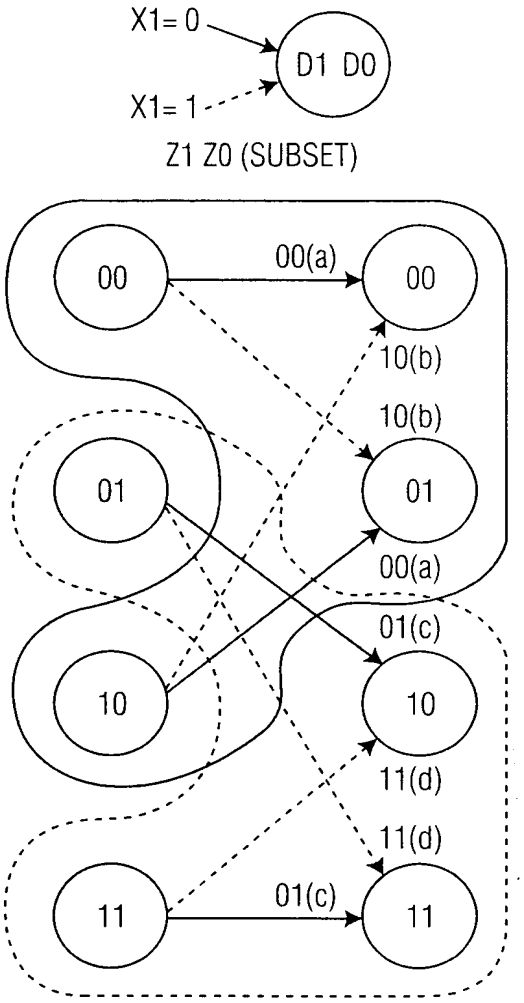


FIG. 5A
PRIOR ART

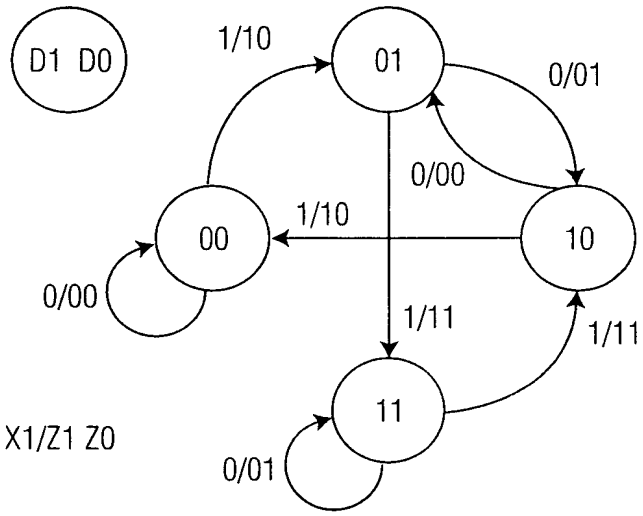


FIG. 5B
PRIOR ART

	PS	NS	
X1	D1 D0	D1 D0	Z1 Z0
0	0 0	0 0	0 0
0	0 1	1 0	0 1
0	1 0	0 1	0 0
0	1 1	1 1	0 1
1	0 0	0 1	1 0
1	0 1	1 1	1 1
1	1 0	0 0	1 0
1	1 1	1 0	1 1

FIG. 5C
PRIOR ART

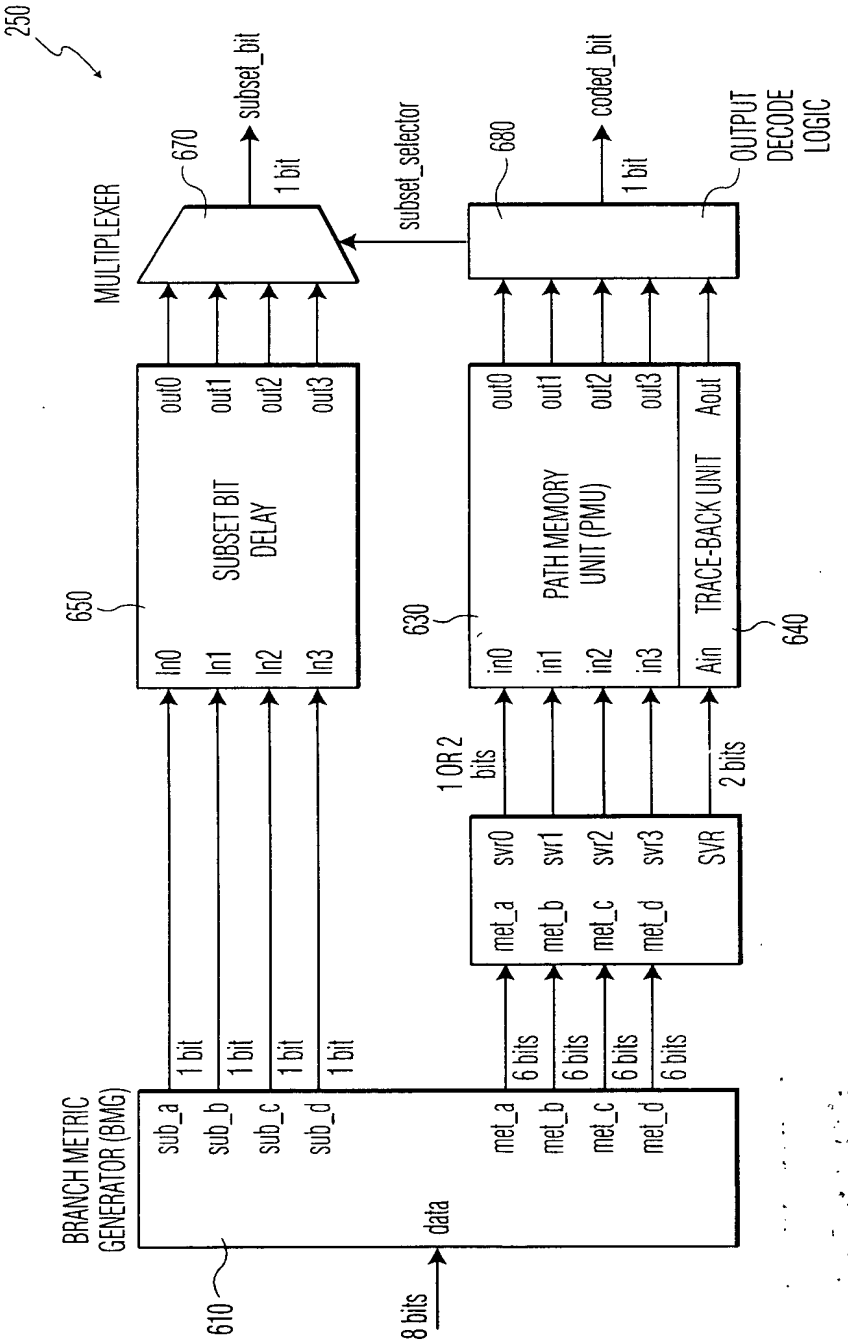


FIG. 6
PRIOR ART

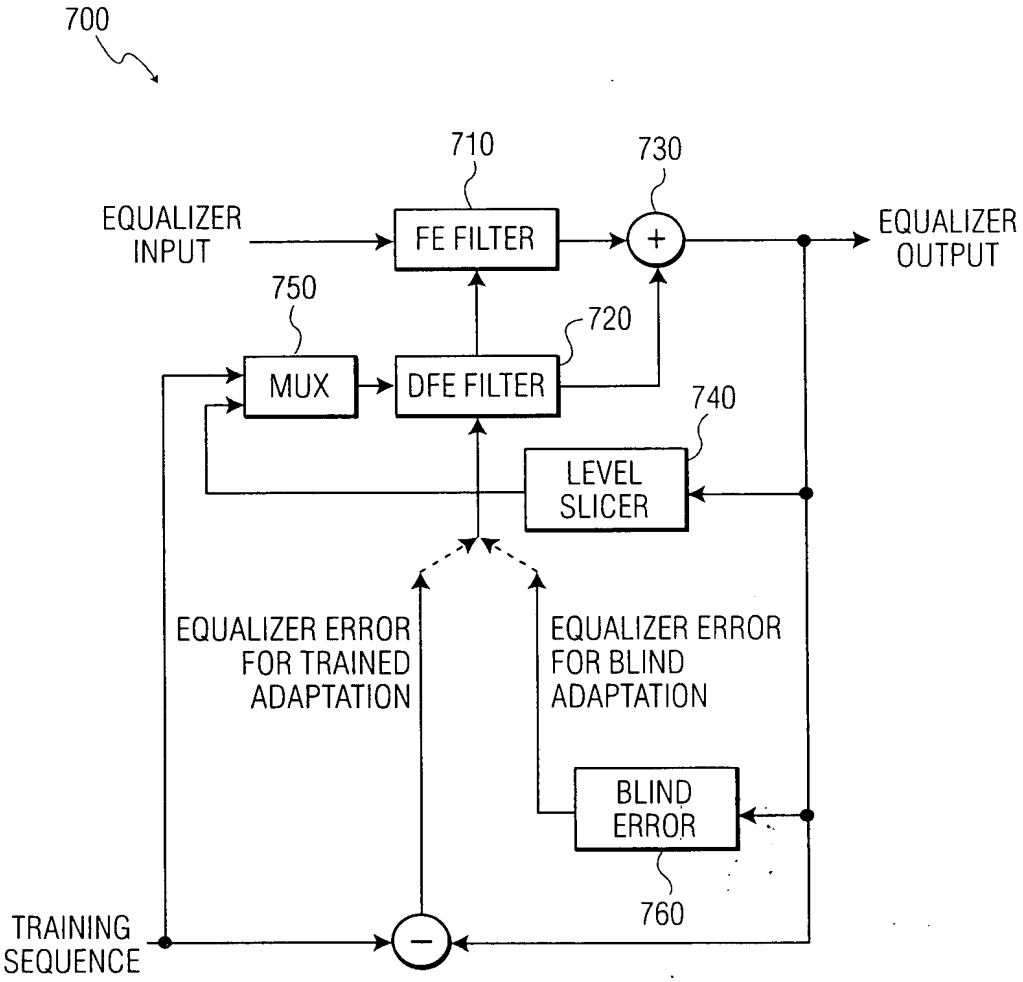
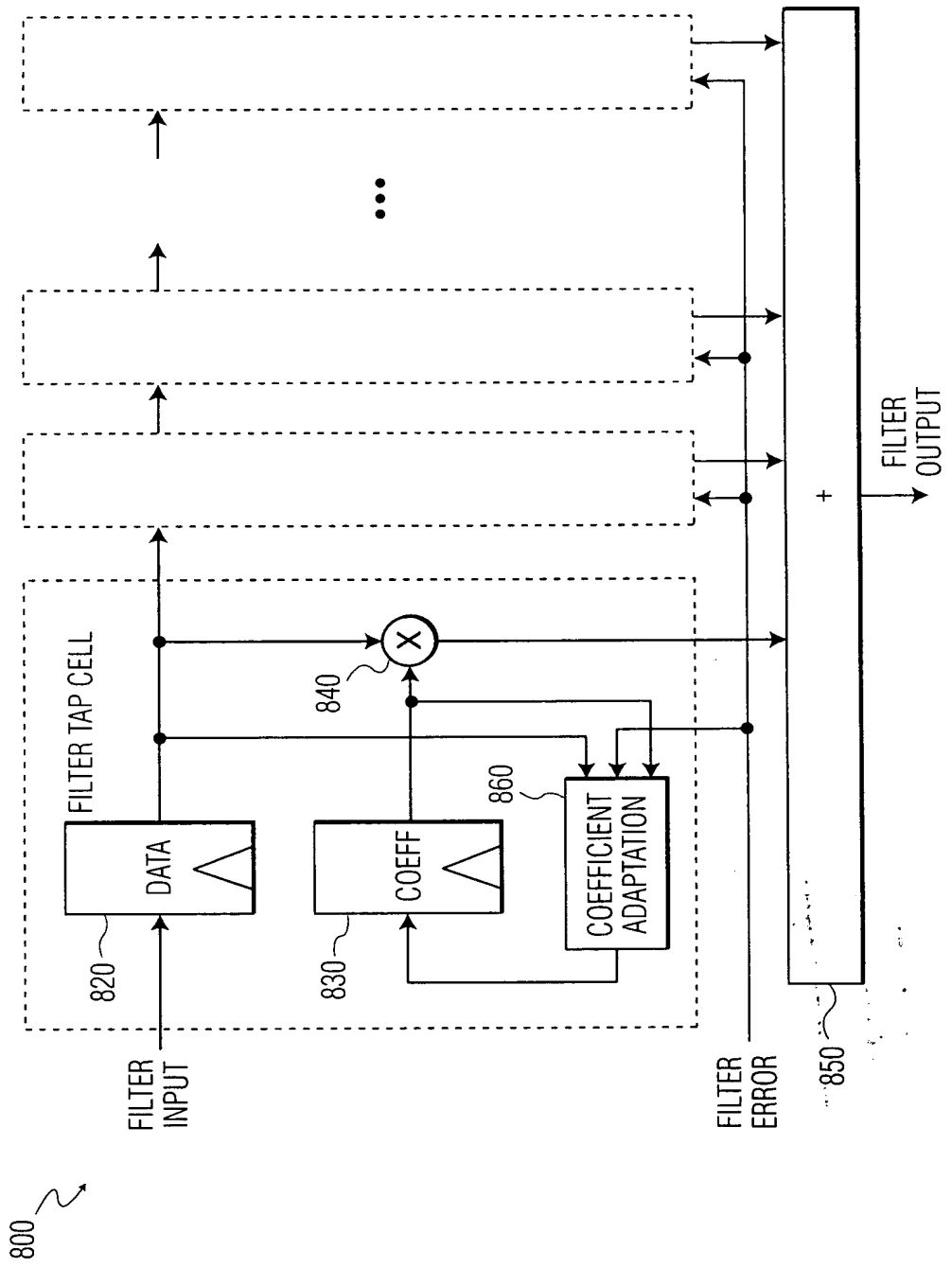


FIG. 7
PRIOR ART

FIG. 8
PRIOR ART



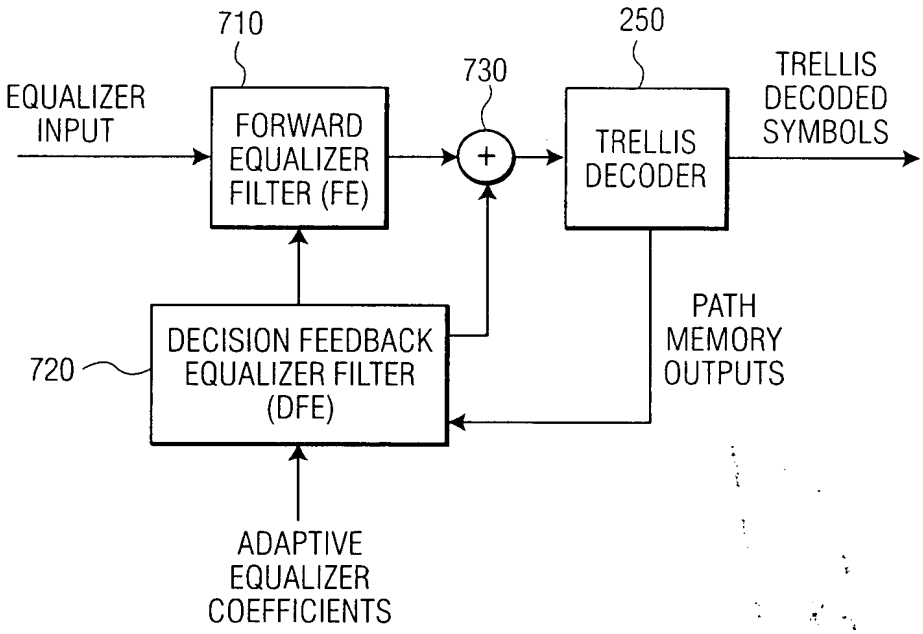

710
250
730
EQUALIZER INPUT
FORWARD EQUALIZER FILTER (FE)
+
TRELLIS DECODER
TRELLIS DECODED SYMBOLS
PATH MEMORY OUTPUTS
720
DECISION FEEDBACK EQUALIZER FILTER (DFE)
ADAPTIVE EQUALIZER COEFFICIENTS

FIG. 9

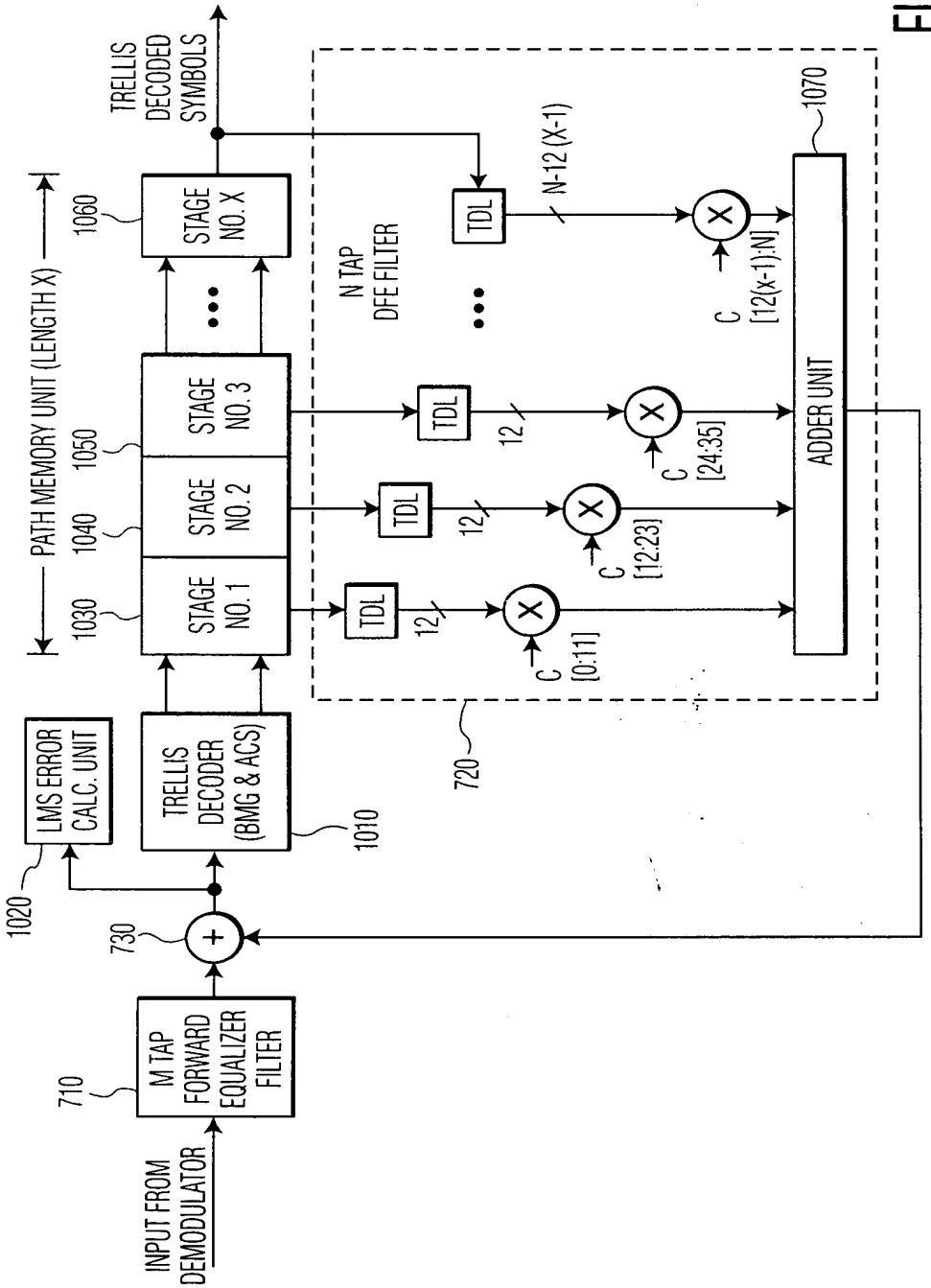

INPUT FROM DEMODULATOR
M TAP FORWARD EQUALIZER FILTER
710
730
1020
LMS ERROR CALC. UNIT
TRELLIS DECODER (BMG & ACS)
1010
PATH MEMORY UNIT (LENGTH X)
STAGE NO. 1
STAGE NO. 2
STAGE NO. 3
STAGE NO. X
1030
1040
1050
1060
TRELLIS DECODED SYMBOLS
N TAP DFE FILTER
720
TDL
12
C [0:11]
C [12:23]
C [24:35]
N-12 (X-1)
C [12(x-1):N]
1070
ADDER UNIT

FIG. 10

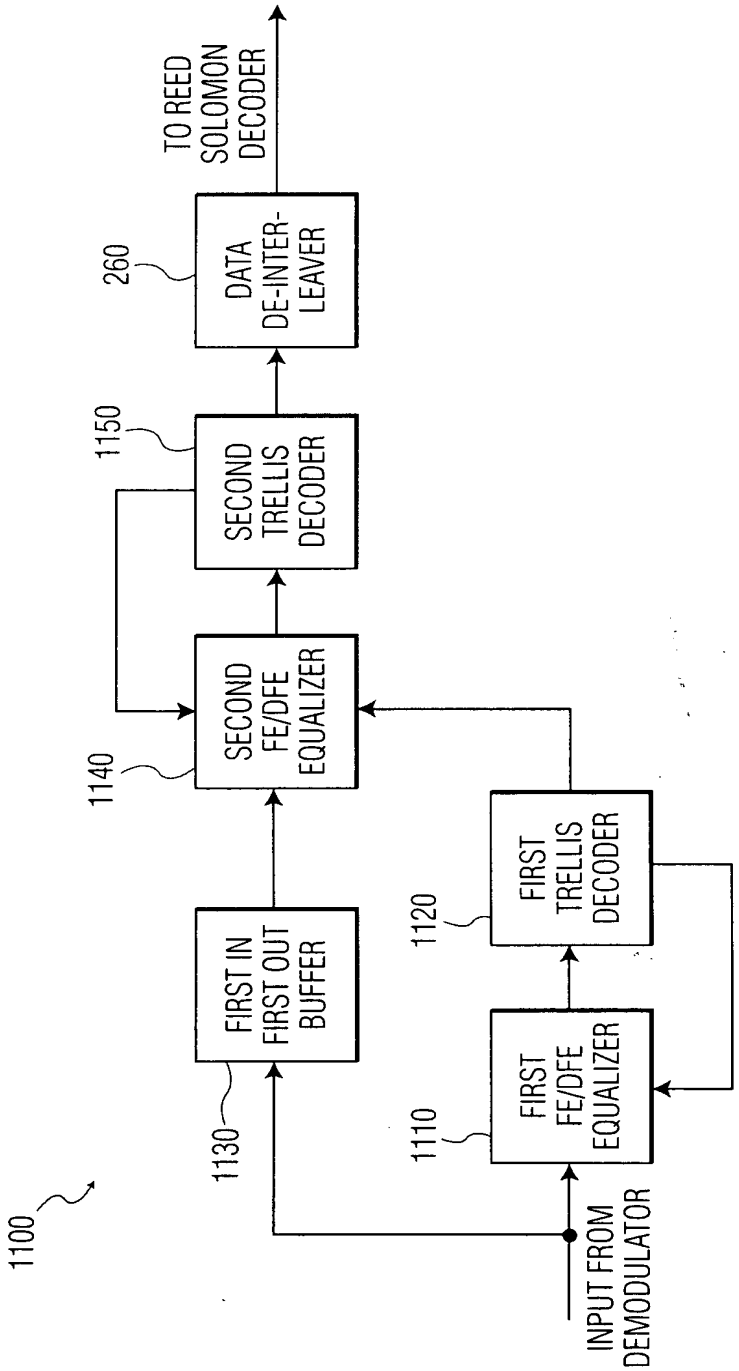

1100
INPUT FROM DEMODULATOR
1110
FIRST FE/DFE EQUALIZER
1120
FIRST TRELLIS DECODER
1130
FIRST IN FIRST OUT BUFFER
1140
SECOND FE/DFE EQUALIZER
1150
SECOND TRELLIS DECODER
260
DATA DE-INTER-LEAVER
TO REED SOLOMON DECODER

FIG. 11

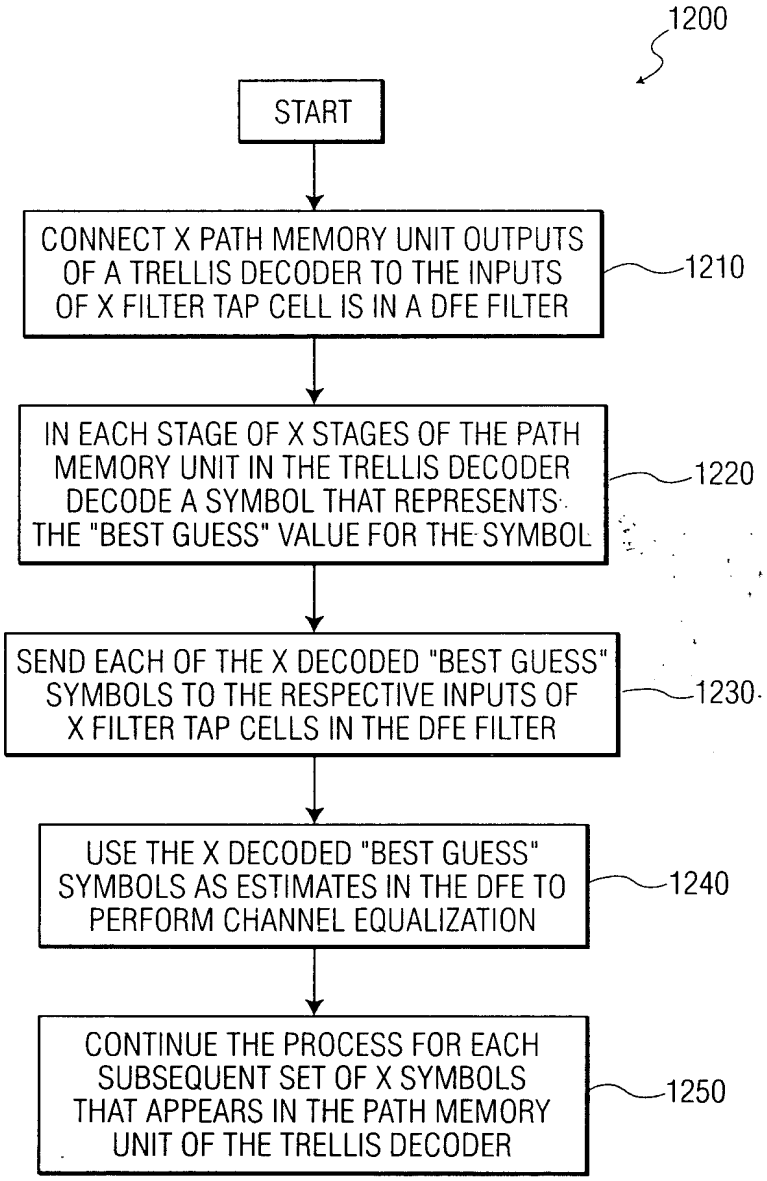
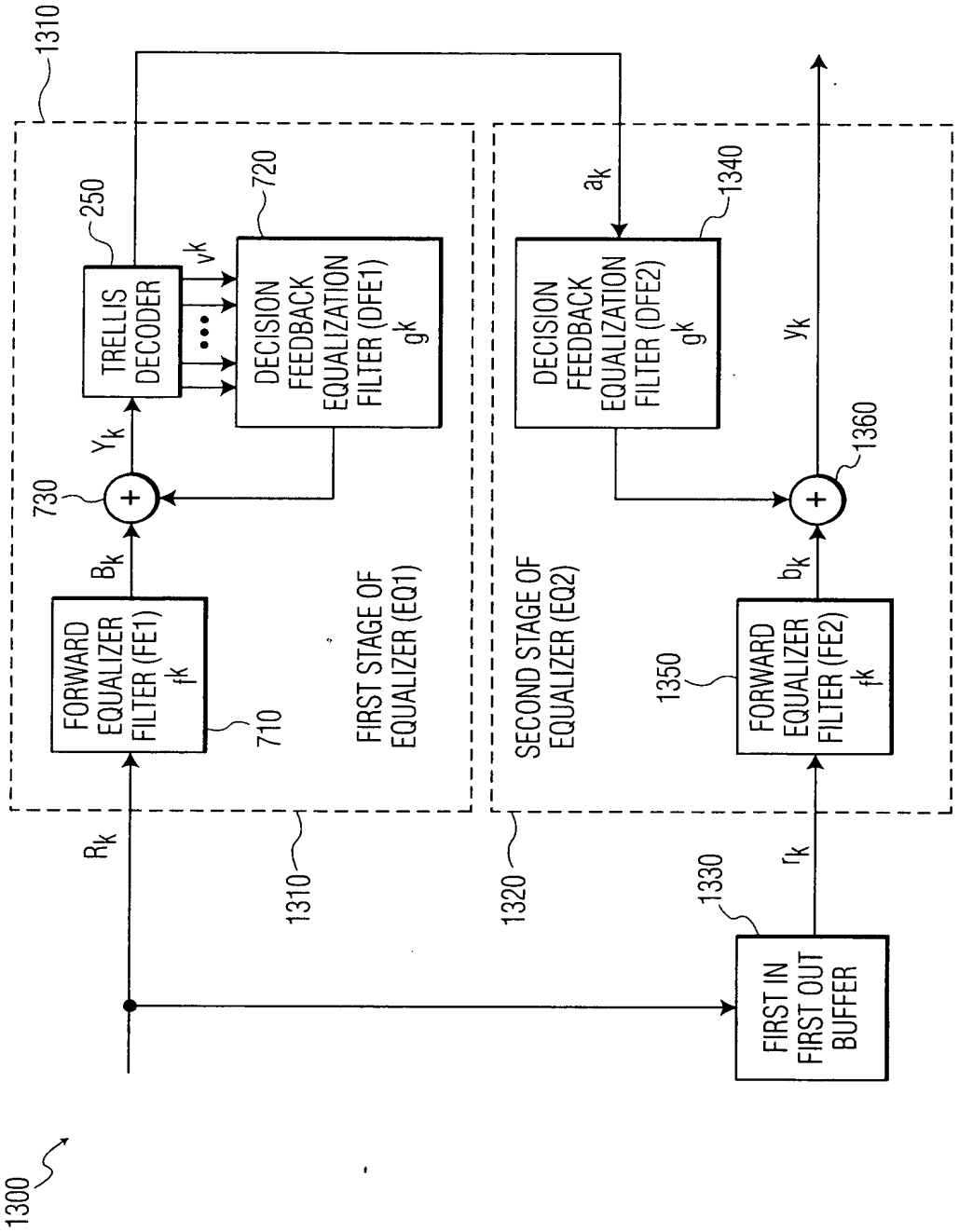

1200
START
CONNECT X PATH MEMORY UNIT OUTPUTS OF A TRELLIS DECODER TO THE INPUTS OF X FILTER TAP CELL IS IN A DFE FILTER
1210
IN EACH STAGE OF X STAGES OF THE PATH MEMORY UNIT IN THE TRELLIS DECODER DECODE A SYMBOL THAT REPRESENTS THE "BEST GUESS" VALUE FOR THE SYMBOL
1220
SEND EACH OF THE X DECODED "BEST GUESS" SYMBOLS TO THE RESPECTIVE INPUTS OF X FILTER TAP CELLS IN THE DFE FILTER
1230
USE THE X DECODED "BEST GUESS" SYMBOLS AS ESTIMATES IN THE DFE TO PERFORM CHANNEL EQUALIZATION
1240
CONTINUE THE PROCESS FOR EACH SUBSEQUENT SET OF X SYMBOLS THAT APPEARS IN THE PATH MEMORY UNIT OF THE TRELLIS DECODER
1250

FIG. 12

FIG. 13


1300
1310
FIRST STAGE OF EQUALIZER (EQ1)
1310
SECOND STAGE OF EQUALIZER (EQ2)
1320
FORWARD EQUALIZER FILTER (FE1) f^k
710
FORWARD EQUALIZER FILTER (FE2) f^k
1350
TRELLIS DECODER
250
DECISION FEEDBACK EQUALIZATION FILTER (DFE1) g^k
720
DECISION FEEDBACK EQUALIZATION FILTER (DFE2) g^k
1340
FIRST IN FIRST OUT BUFFER
1330
730
1360
R_k
B_k
Y_k
v^k
a_k
y_k
b_k
r_k

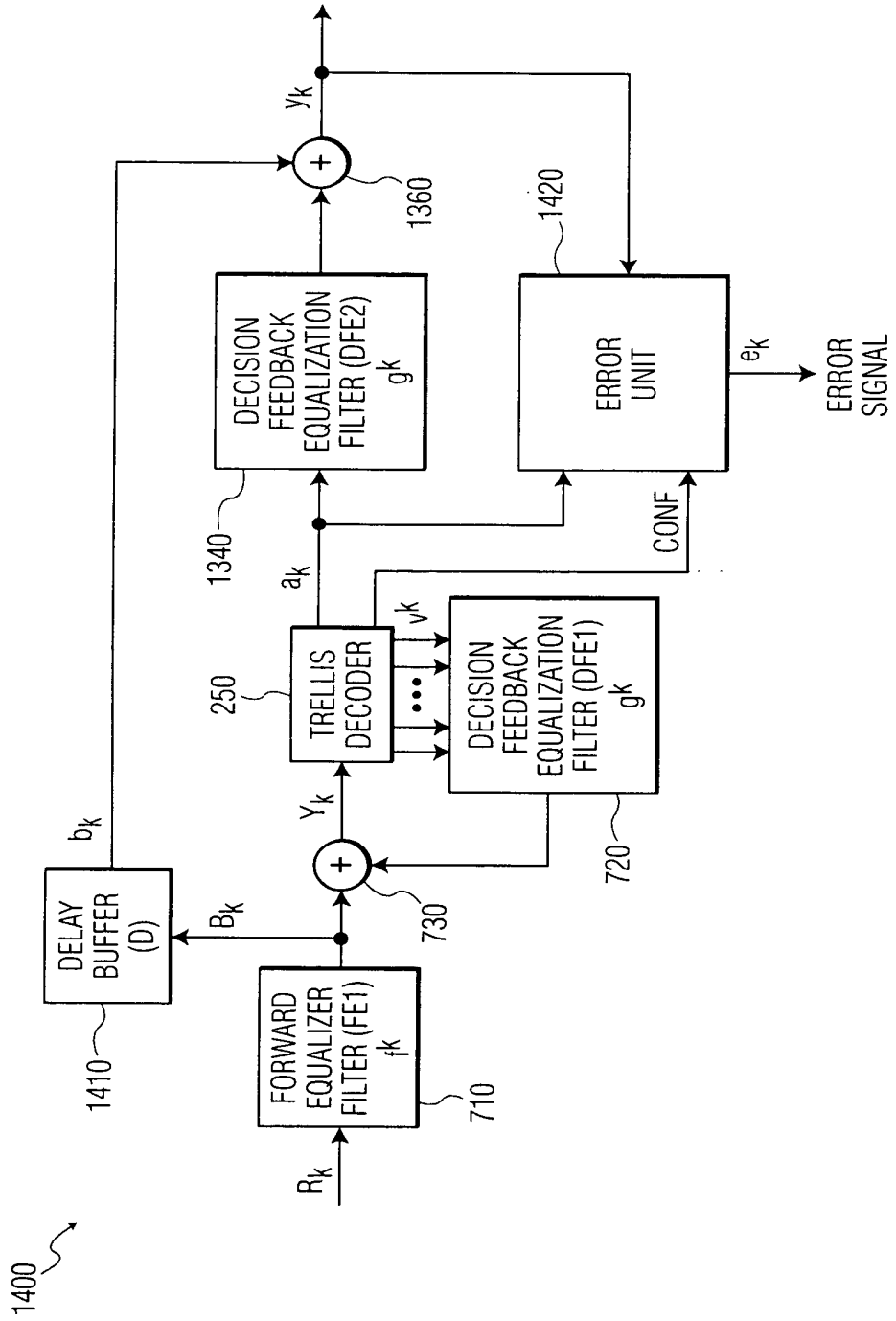

1400
1410
DELAY BUFFER (D)
b_k
B_k
FORWARD EQUALIZER FILTER (FE1) f^k
710
R_k
730
Y_k
TRELLIS DECODER
250
v^k
DECISION FEEDBACK EQUALIZATION FILTER (DFE1) g^k
720
a_k
1340
DECISION FEEDBACK EQUALIZATION FILTER (DFE2) g^k
1360
y_k
1420
ERROR UNIT
CONF
e_k
ERROR SIGNAL

FIG. 14

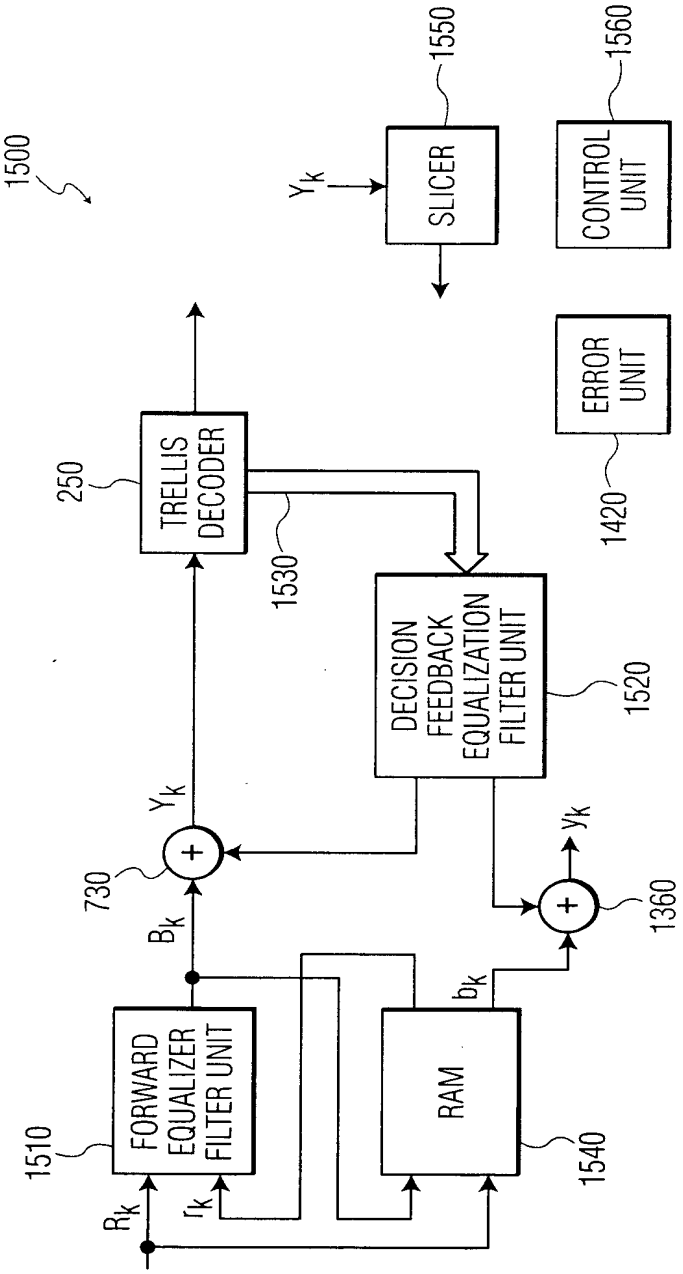

1500
Y_k
SLICER
1550
CONTROL UNIT
1560
ERROR UNIT
1420
250
TRELLIS DECODER
1530
DECISION FEEDBACK EQUALIZATION FILTER UNIT
1520
Y_k
730
B_k
y_k
1360
b_k
1510
FORWARD EQUALIZER FILTER UNIT
RAM
1540
R_k
r_k

FIG. 15